What is Claimed is:

1. An apparatus for encoding a DSL information bit stream comprising:

a switch having an input configured to receive a DSL information bit stream and at least two outputs, including a first switch output and a second switch output;

a first encoder having an input coupled to the first switch output;

a serial to parallel converter coupled to both an output of the first encoder and the second switch output;

a mapper coupled to an output of the serial to parallel converter through multiple paths, wherein a first coupling path is a direct path and a second coupling path includes a second encoder.

2. The apparatus of claim 1, wherein the first encoder is a Reed-Solomon encoder.

3. The apparatus of claim 1, wherein the second encoder is a block turbo encoder.4. The apparatus of claim 1, wherein the second encoder is a convolutional turbo encoder.5. An apparatus for encoding a DSL information bit stream comprising:

a switch having an input configured to receive a DSL information bit stream and at least two outputs, including a first switch output and a second switch output;

a first encoder having an input coupled to the first switch output; and

a serial to parallel converter coupled to both an output of the first encoder and the second switch output.

6. The apparatus of claim 5, wherein the first encoder is a Reed-Solomon encoder.

7. The apparatus of claim 5, further including an interleaver interposed between the first encoder and the serial to parallel converter.

8. The apparatus of claim 5, further including a mapper directly coupled to an output of the serial to parallel converter.

9. The apparatus of claim 8, further including a second encoder interposed between the serial to parallel converter and the mapper.

10. The apparatus of claim 9, wherein the second encoder is a concatenated encoder.

11. The apparatus of claim 9, wherein the second encoder is a turbo coder.

12. The apparatus of claim 11, wherein the turbo coder is a block turbo coder.

13. The apparatus of claim 11, wherein the turbo coder is a convolutional turbo coder.

14. The apparatus of claim 5, further including a third encoder interposed between the second switch input and the serial to parallel converter.

15. The apparatus of claim 5, further including a controller for controlling the operation of the switch based upon the latency of the DSL information bit stream.

16. An apparatus for encoding a DSL information bit stream comprising:

a switch having an input configured to receive a DSL information bit stream and at least three outputs;

a plurality of encoders, each encoder coupled to a different output of the switch and each encoder defined by a different interleaving depth;

a serial to parallel converter coupled to an output of each of the plurality of encoders.

17. The apparatus of claim 16, wherein the serial to parallel converter is also coupled directly to one of the switch outputs.

18. The apparatus of claim 16, wherein each of the plurality of encoders are Reed-Solomon encoders.

19. A method for encoding a DSL information bit stream comprising:

providing at least two paths between an input configured to receive the DSL information bit stream and a serial to parallel converter;

providing a first encoder in one of the at least two paths; and

switching the DSL information bit stream through one of the at least two paths based upon a latency in the DSL information bit stream.

20. An apparatus for decoding an encoded DSL symbol comprising:

a soft demapper configured to generate multiple outputs, including an uncoded bit stream having an input configured to receive a DSL information bit stream and at least one coded bit stream;

at least one decoder configured to decode the at least one coded bit stream; and

a circuit configured to perform a hard demapping of both the uncoded bit stream and an output of the at least one decoder.

21. The apparatus of claim 20, further including a deinterleaver configured to operate on an output of the hard demapper corresponding to a demapping of the uncoded bit stream.

22. The apparatus of claim 21, further including an Reed-Solomon decoder configured to decode an output of the deinterleaver.

23. The apparatus of claim 20, wherein the circuit is implemented primarily through dedicated hardware.

24. The apparatus of claim 20, wherein the circuit is implemented through general purpose hardware that is micro-coded with instructions to carry out the demapping function.